Amendments to the Claims:

Listing of Claims:

Claim 1 (currently amended): A circuit comprising:

an operational amplifier comprising a positive input end, a negative input end, and an output end;

a first input impedance coupled between the negative input end and a first input signal;

a second input impedance coupled between the negative input end and a second input signal; and

a first output impedance coupled between the negative input end and the output end [[,]];

wherein resistances of the first and second input impedances are controlled by a first and a second control signals respectively, so that the resistances of the first and second impedances are substantially different from each other.

Claim 2 (original): The circuit of claim 1 wherein resistances of the first and second input impedances are close to each other.

Claim 3 (original): The circuit of claim 2 wherein the circuit has a high input impedance characteristic.

Claim 4 (original): The circuit of claim 2 wherein the first output impedance is a resistive-impedance, the circuit has a high voltage attenuation characteristic.

Claim 5 (original): The circuit of claim 2 wherein the first output impedance is a capacitive-impedance, the circuit has a large time constant characteristic.

Claim 6 (original): The circuit of claim 1 wherein the first input impedance is a switched capacitor circuit, the switched capacitor circuit comprises:

a capacitor coupled between a first node and a ground end;

a first switch with one end coupled to the first node and another end used as an end of the switched capacitor circuit; and

a second switch with one end coupled to the first node and another end used as another end of the switched capacitor circuit,

wherein the first switch and the second switch are turned on alternately by the first control signal.

Claim 7 (currently amended): A circuit comprising:

a differential amplifier comprising a positive input end, a negative input end, a positive output end, and a negative output end;

a first input impedance coupled between the negative input end and a first input signal;

a second input impedance coupled between the positive input end and the first input signal;

a third input impedance coupled between the negative input end and a second input signal, the third input impedance being substantially equivalent to the second input impedance; and

a fourth input impedance coupled between the positive input end and the second input signal, the fourth input impedance being substantially equivalent to the first input impedance;

wherein resistances of the first and second input impedances are controlled by a first and a second control signals respectively.

Claim 8 (original): The circuit of claim 7 wherein resistances of the first and second input impedances are close to each other.

Claim 9 (original): The circuit of claim 8 wherein the circuit has a high input impedance characteristic.

Claim 10 (original): The circuit of claim 7 further comprising:

a first output impedance coupled between the negative input end and the positive output end; and

a second output impedance coupled between the positive input end and the negative output end.

Claim 11 (original): The circuit of claim 10 wherein the first and the second output impedances are a resistive-impedance, the circuit has a high voltage attenuation characteristic.

Claim 12 (original): The circuit of claim 10 wherein at least one the first and the second output impedance is a capacitive-impedance, the circuit has a large time constant characteristic.

Claim 13 (original): The circuit of claim 7 wherein the first input impedance is a switched capacitor circuit, the switched capacitor circuit comprises:

a capacitor coupled between a first node and a ground end;

a first switch with one end coupled to the first node and another end used as an end of the switched capacitor circuit; and

a second switch with one end coupled to the first node and another end used as another end of the switched capacitor circuit,

wherein the first switch and the second switch are turned on alternately by the first control signal.

Claim 14 (original): A circuit comprising:

a differential amplifier comprising a positive input end, a negative input end, a positive output end, and a negative output end;

a first input impedance coupled between the negative input end and a first input signal;

a second input impedance coupled between the positive input end and the second input signal;

a first output impedance coupled between the negative input end and the positive output end;

a second output impedance coupled between the negative input end and the negative output end;

a third output impedance coupled between the positive input end and the positive output end, the third output impedance being substantially equivalent to the second output impedance; and

a fourth output impedance coupled between the positive input end and the negative output end, the fourth output impedance being substantially equivalent to the first output impedance,

wherein resistances of the first and second output impedances are controlled by a first and a second control signals respectively.

Claim 15 (original): The circuit of claim 14 wherein resistances of the first and the second output impedance are close to each other.

Claim 16 (original): The circuit of claim 15 wherein the first and the second input impedance is a resistive-impedance, the circuit has a high voltage gain characteristic.

Claim 17 (original): The circuit of claim 15 wherein at least one the first and the second input impedance is a capacitive-impedance, the circuit has a large time constant characteristic.

Claim 18 (original): The circuit of claim 14 wherein the first output impedance is a switched capacitor circuit, the switched capacitor circuit comprises:

a capacitor coupled between a first node and a ground end;

a first switch with one end coupled to the first node and another end used as an end of the switched capacitor circuit; and

a second switch with one end coupled to the first node and another end used as another end of the switched capacitor circuit,

wherein the first switch and the second switch are turned on alternately by the first control signal.

Claim 19 (currently amended): [[An]] A circuit comprising:

a differential amplifier comprising a positive input end, a negative input end, a positive output end, and a negative output end;

a first input impedance coupled between the negative input end and a first input signal;

a second input impedance coupled between the positive input end and the first input signal;

a third input impedance coupled between the negative input end and a second input signal, the third input impedance being substantially equivalent to the second input impedance;

a fourth input impedance coupled between the positive input end and the second input signal, the fourth input impedance being substantially equivalent to the first input impedance;

a first output impedance coupled between the negative input end and the positive output end;

a second output impedance coupled between the negative input end and the negative output end;

a third output impedance coupled between the positive input end and the positive output end, the third output impedance being substantially equivalent to the second output impedance; and

a fourth output impedance coupled between the positive input end and the negative output end, the fourth output impedance being substantially equivalent to the first output impedance,

wherein the positive output end is for outputting a first output signal, and the negative output end is for outputting a second output signal.

Claim 20 (currently amended): The ~~amplifying~~ circuit of claim 19 wherein the first input impedance, the second input impedance, the third input impedance, the fourth input impedance, the first output impedance, the second output impedance, the third output impedance, or the fourth output impedance is a switched capacitor circuit.

Claim 21 (new): The circuit of claim 7 wherein the resistances of the first and second input impedances are so controlled by the first and the second control signals respectively, that they are substantially different from each other.

underlying circuit benefits from a high input impedance characteristic. Such claim limitations have never been taught in the cited reference of Gulati, and therefore the amended claim 1 has overcome the rejection under 35 USC 102.

Since amended claim 1 is found allowable, claims 2 – 6 dependent thereupon should also be considered allowable.

Claims 7, and 8 – 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Kuttner U.S. patent No. 6,707,405.

Response:

The Applicants maintain that Kuttner fails to teach or suggest at least the following claim limitation of "the third input impedance being substantially equivalent to the second input impedance," as well as "the fourth impedance being substantially equivalent to the first input impedance." After careful examination of the content of Kuttner, the Applicants are unable to identify any portion of the disclosure that even remotely connects to such claim limitations. Even with the description recited by the Examiner at column 5, lines 46 – 50, Kuttner merely states that "the resistance values of the resistors R6, R7, R8, and R9 correspond with the resistance value of the resistor R4 and the resistor R5." As to how these resistors R6 – R9 correspond with R4 and R5, Kuttner remains silent. In addition, Kuttner merely discloses utilizing switches S6-S9 to control signal paths (col. 5, lines 56-65). There is no disclosure stating that the input impedances are controlled by control signals applied to the switches S6 – S9. In short, Kuttner fails to teach or suggest controlling the input impedances by control signals.

As a result, the Applicants are reluctant to believe that these claimed limitations are properly anticipated, or made obvious, by Kuttner. Therefore, the independent claim 7 should be considered allowable.

Since amended claim 7 is found allowable, claims 8 – 11 dependent thereupon should also be considered allowable.

Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gulati et al. as applied to claim 2 above.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuttner, in view of Gulatio et al. as applied to claim 2 above, in view of Sobel U.S. Patent 6,833,759.

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuttner, in view of Gulatio et al. as applied to claim 5 above.

Response:

Since claims 3 – 5 and 12 – 13 are dependent claims of either the independent claim 1 or 7, they should also be considered allowable for at least one of the above detailed reasons.

New claim 21

The new claim 21 is a dependent claim of the independent claim 7, so it should be found allowable for at least the same reason claim 7 is being deemed allowable. In addition, claim 21 further recites the limitation of substantially different resistances of the first impedance

and the second impedance, which is never taught by any of the cited references.

Allowable Subject Matter

As stated by Examiner in this office action, Claim 14 – 20 are allowed. Since claims 19 & 20 are amended only for grammatical error and typographical error, the amended claims 19 & 20 remain allowable.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)